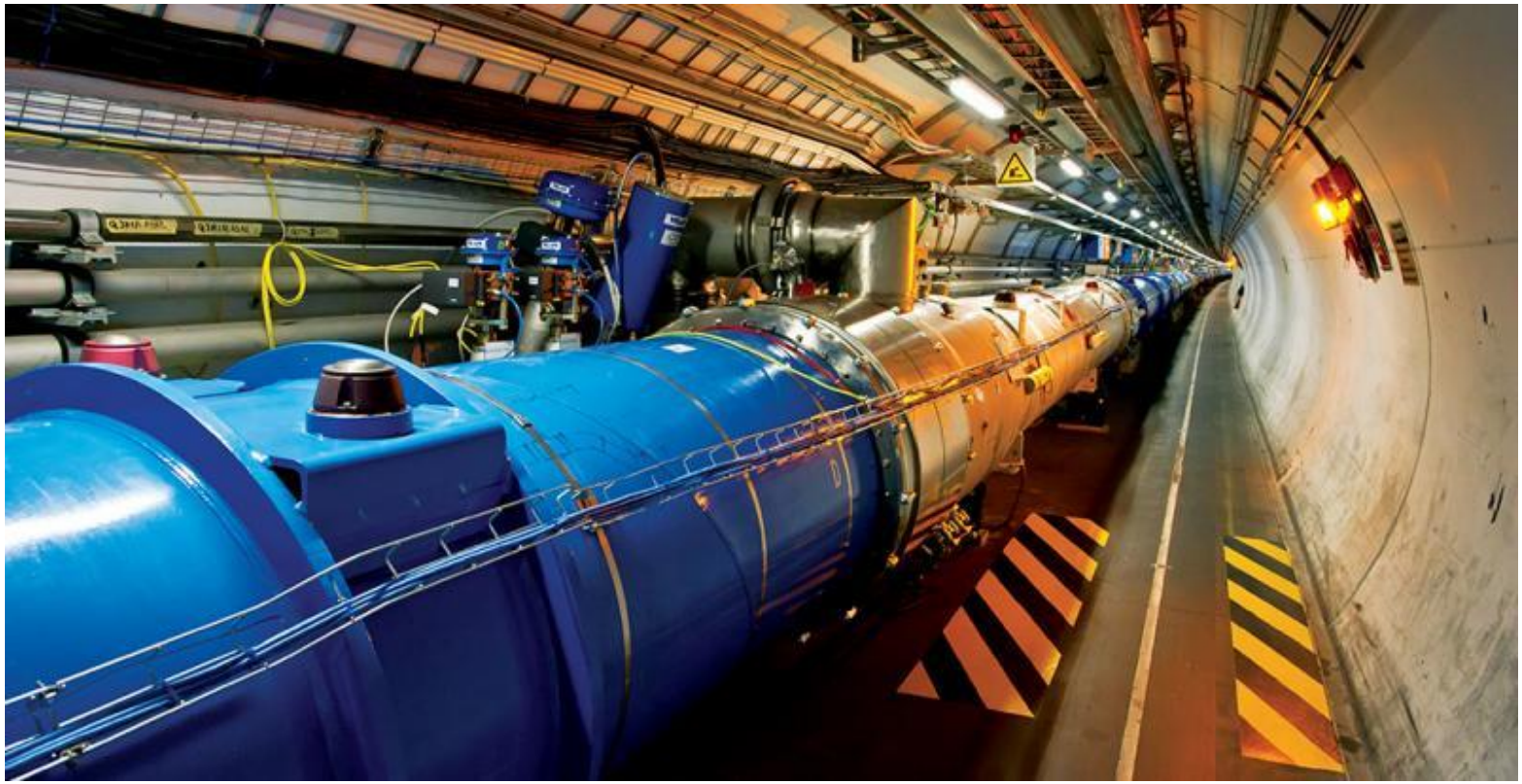

High DR ADC for LHC

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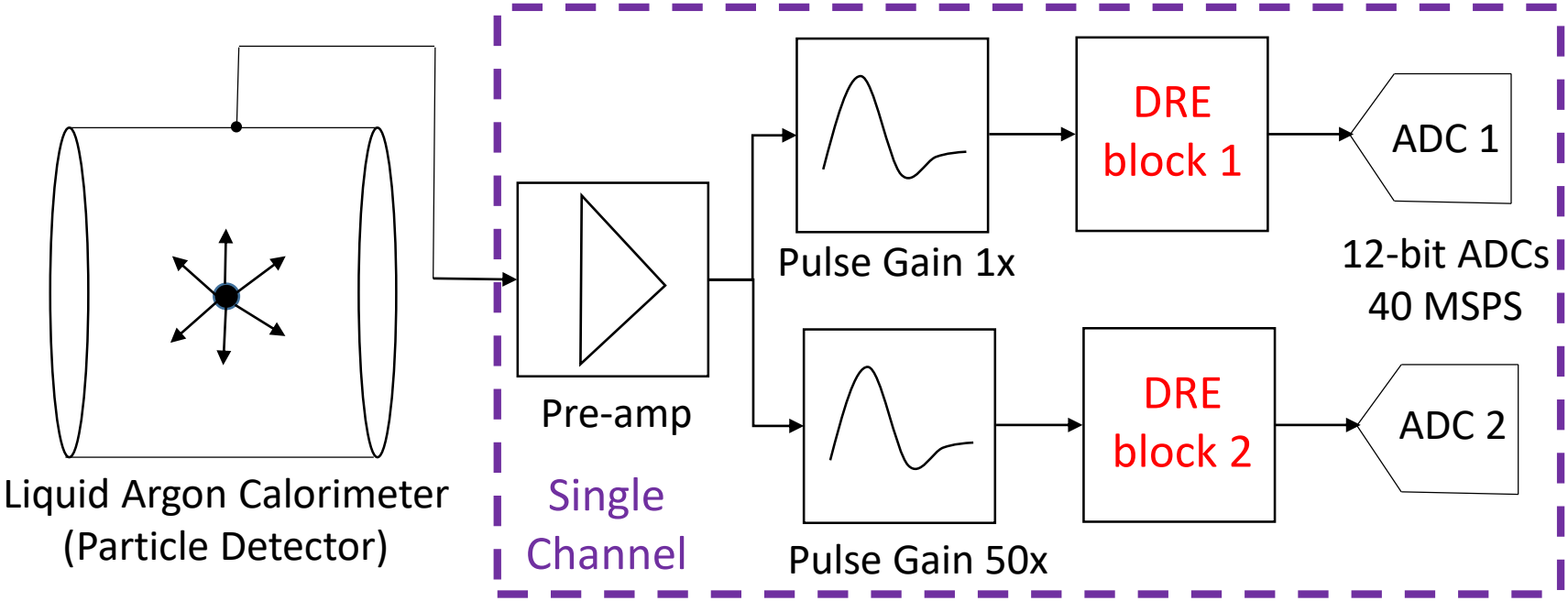
Last updated: 12/01/16

COLUMBIA UNIVERSITY
IN THE CITY OF NEW YORK

Columbia Integrated Systems Laboratory

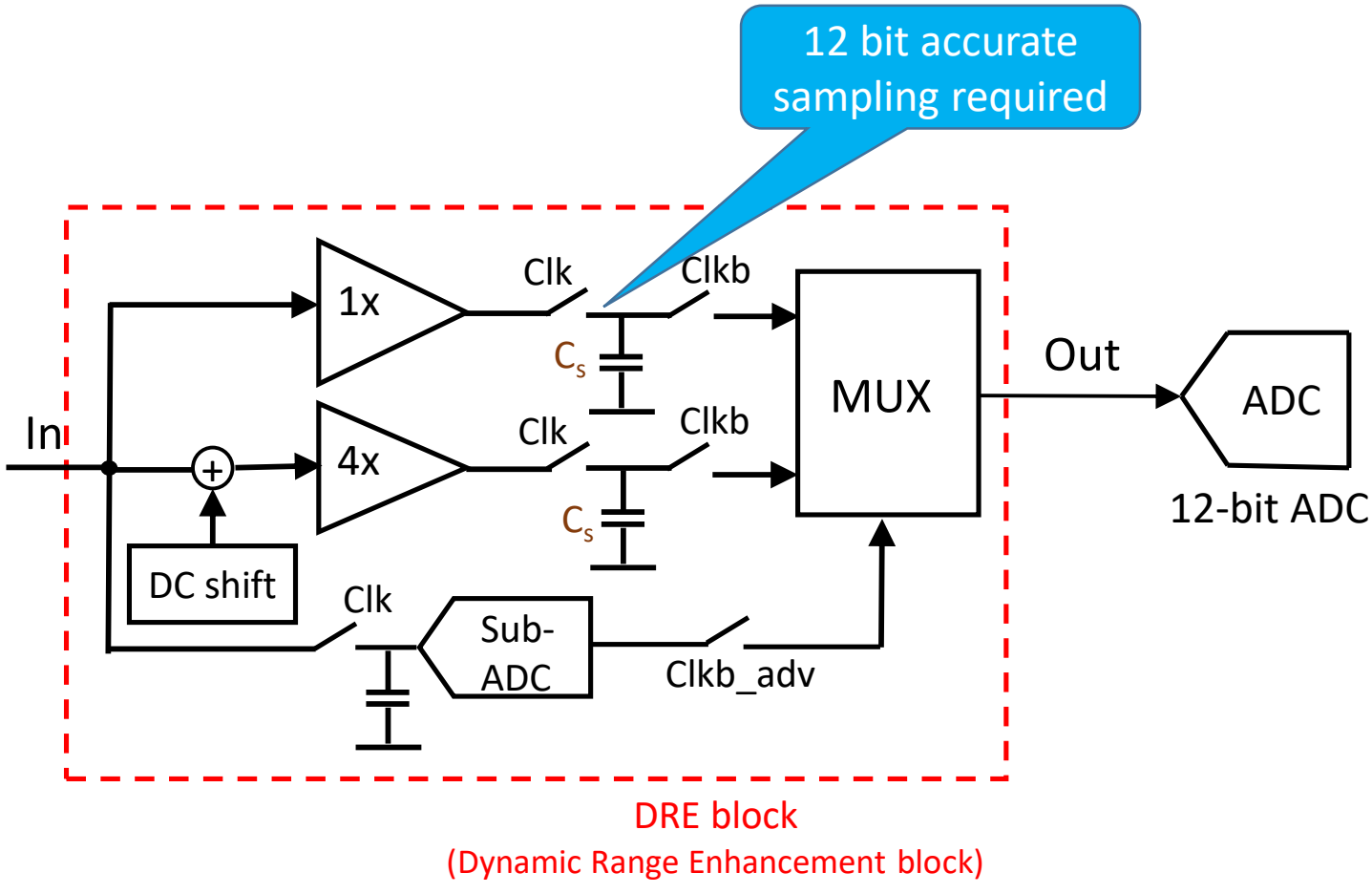
Aim: ADC design for The LHC (Large Hadron Collider), CERN

- ADC specifications:
  - 14-bit design: To accommodate high dynamic range (16 bit)
  - 40MSps
- To design: intermediate block
  - Increase accuracy to 14 bit (or enhance the dynamic range)



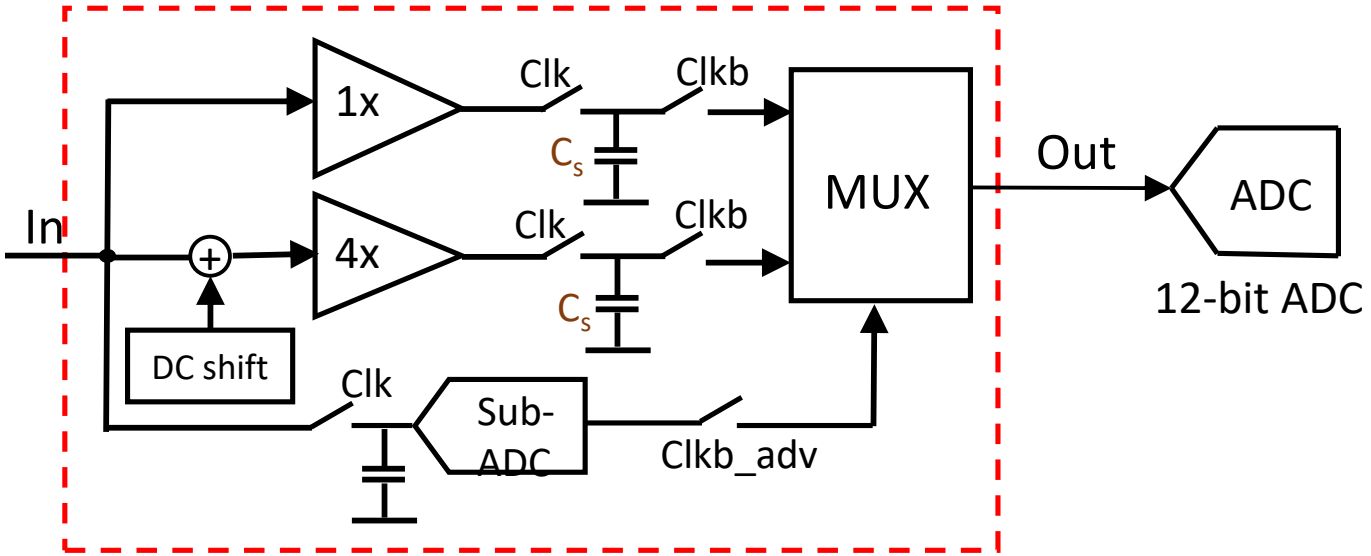
Proposed architecture: Concept

12-bit accurate sampling after analog gain
& dc shift for 4x gain



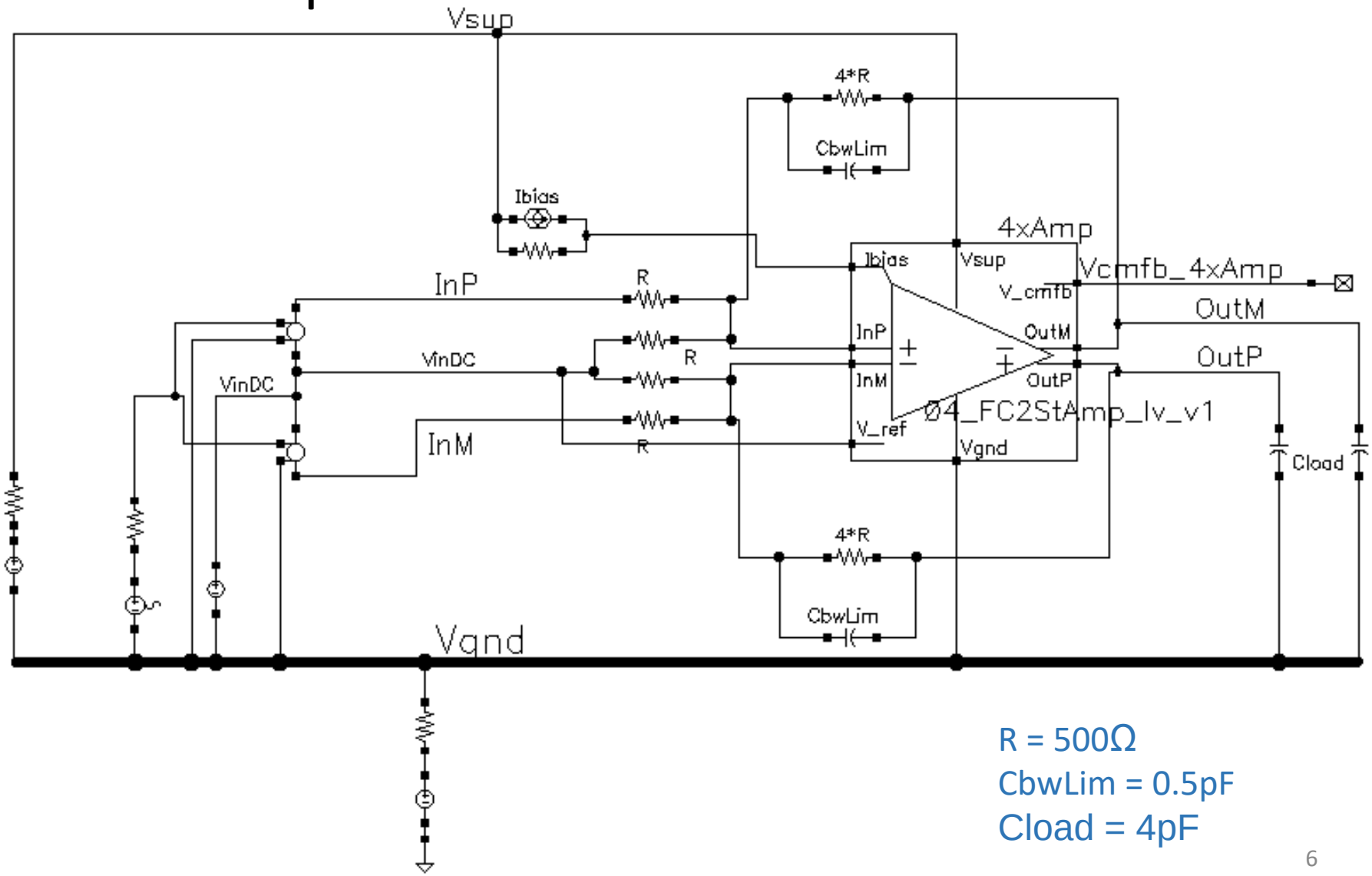
4x branch assumption

- **Calibration**
  - Exact values for 1x and 4x might not matter (Similar to gain error?)
  - 1x and 4x branch inter-calibration can be done similar to interstage calibration in Nevis 2013 design.



4x Amplifier design

4x Amplifier Testbench



R = 500Ω
CbwLim = 0.5pF
Cload = 4pF

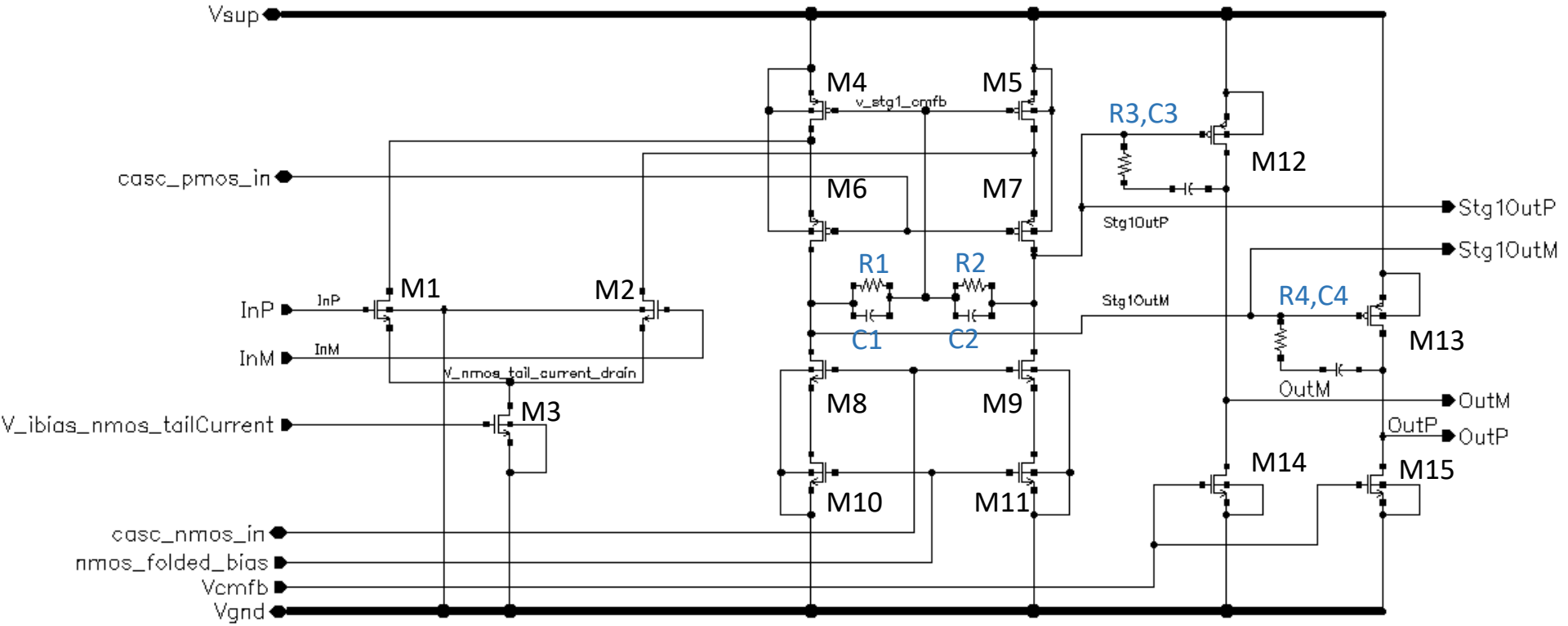
4x Amplifier Requirements

Requirement	Value	Comments	Challenges
Voltage Swing	$2V_{PP}$ differential	Determined by amplifier 2^{nd} stage (Affects THD)	THD requirement limits max swing
THD	>76dB	Both noise and distortion should be -76dBV (or less) to have SNDR of 73dB atleast (Signal is 0dBV for peak voltage)	Tradeoff with Voltage swing. Might need different architecture
Noise	< $100uV_{RMS}$	Peak RMS voltage = 0.707V, and noise RMS should be 76dB down.	Need to optimize bandwidth and noise
Band width	>60MHz	A signal of 20MHz should have gain close to 4x.	Noise and power tradeoff
Cload	4pF single ended	Sampling Cap load	

4x Amplifier Requirements (contd.)

Requirement	Value	Comments	Challenges
Loop gain	>76dB Or as high as possible	>76 dB will mean no calibration needed. Not possible. So practically, after a feedback factor of 1/9 we get about 44dB loop gain	Feedback factor, Resistance value to be driven
Feed-back factor	1/9	(See schematic)	Reduces DC loop gain, bandwidth.

4x Amplifier schematic



M1,M2 = 40u/240n
M3 = 80u/240n

M4,M5 = 160u/240n
M6, M7 = 240u/240n
M8,M9 = 120u/240n
M10, M11 = 40u/240n

M12,M13 = 160u/240n
M14,M15 = 80u/240n

Cload = 4pF

R1,R2 = 200kΩ
R3,R4 = 60Ω
C1,C2 = 1pF
C3,C4 = 1pF

Current amplifier status

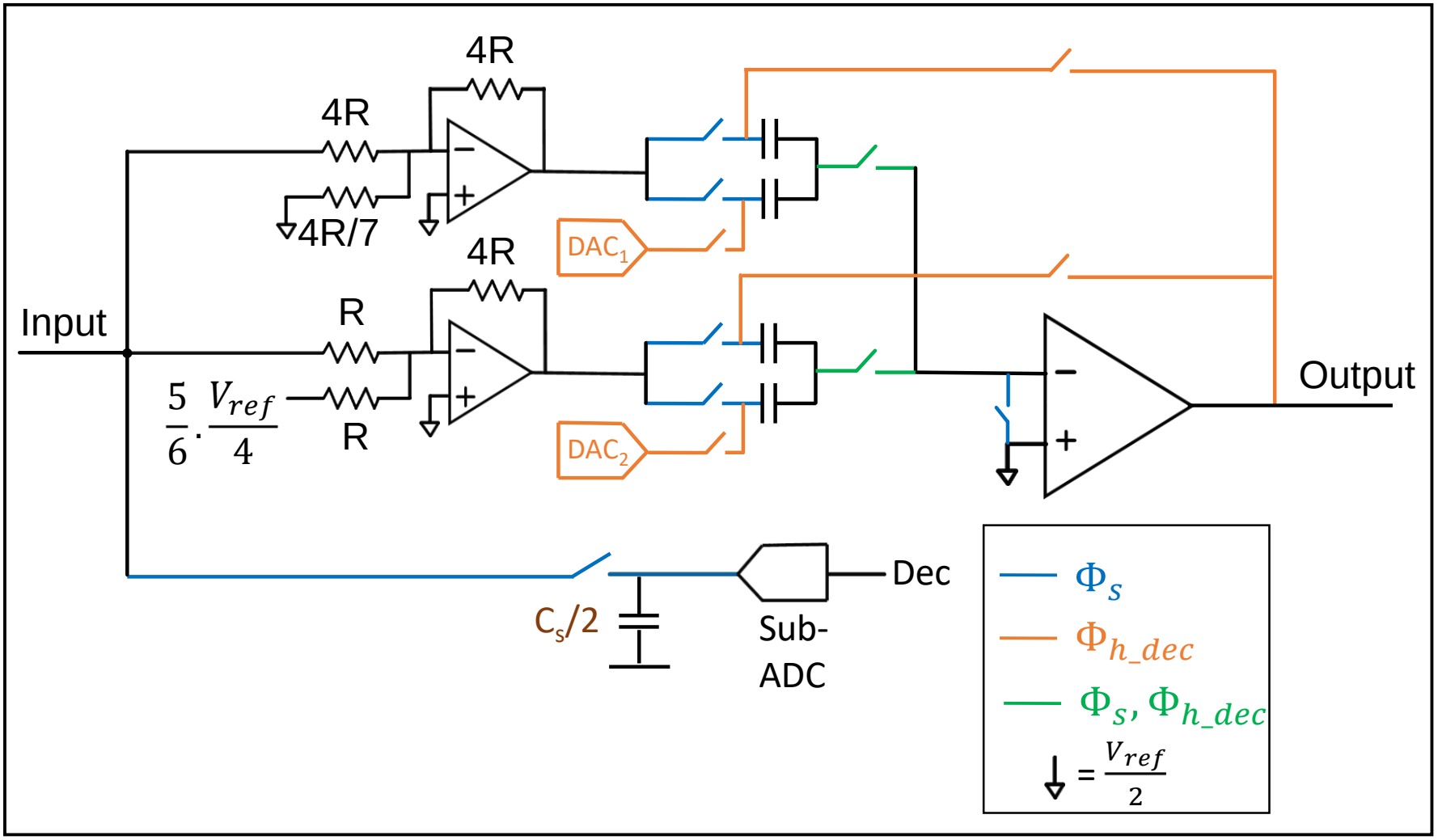
	Simulated Value	Required Value	Comment/Plan to improve
DC Loop Gain	44dB	76dB	Need calibration scheme for interstage calibrations
UGB	86MHz	80MHz	
Noise	$472uV_{RMS}$	$100uV_{RMS}$	Transistor resizing, increasing 1^{st} stage current, using capacitor parallel to feedback resistor to suppress resistor noise
Phase Margin	76^0	60^0	
3^{rd} Harmonic @$1V_{pp}$ diff	80dB	76dB	(simulated at low frequency: 97/1024MHz)
3^{rd} Harmonic @$2V_{pp}$ diff	50dB	76dB	Use a different architecture?
Power	1.2V*4.2mA	<10mW	

Further plans

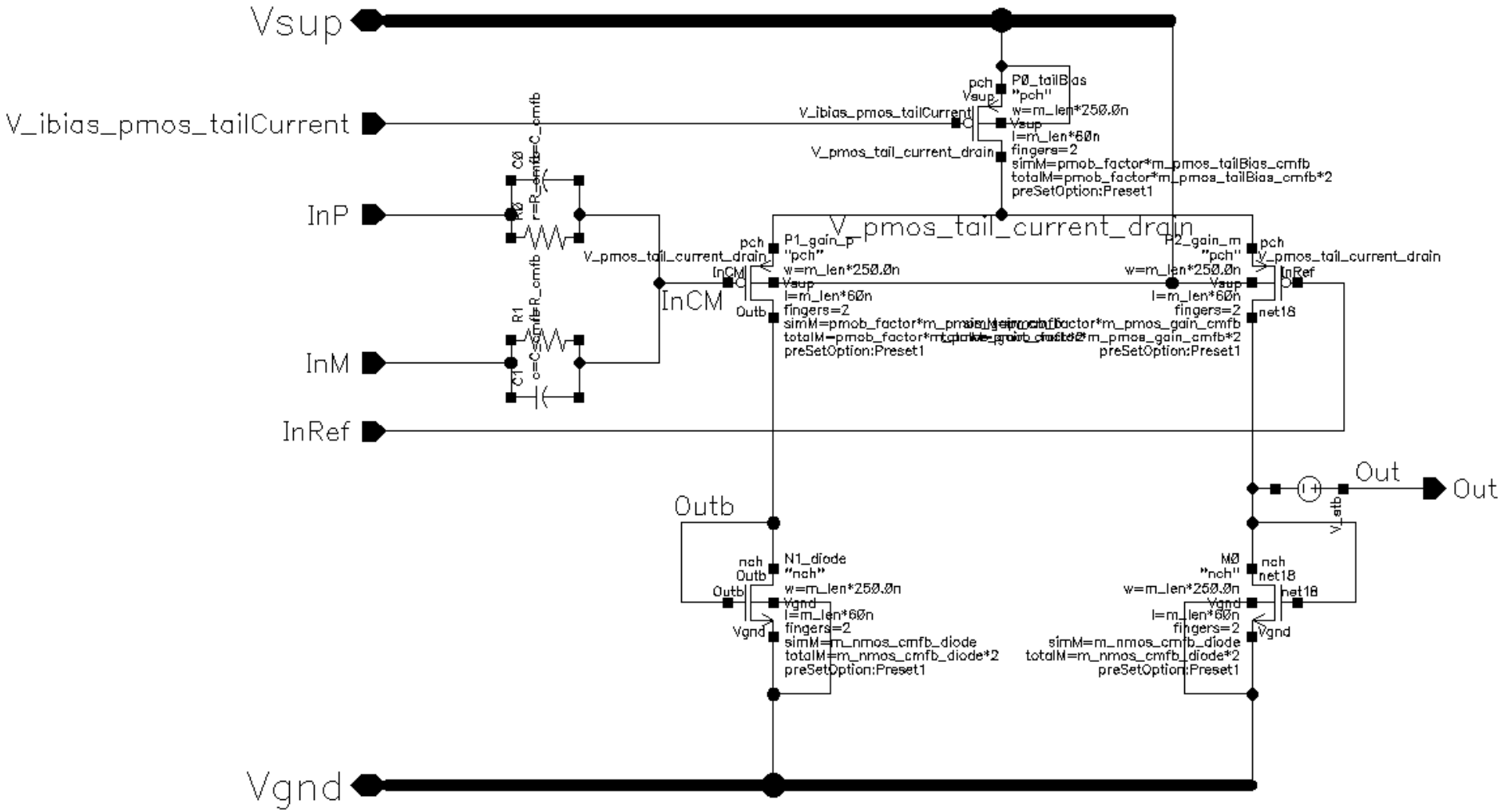
- Reduce noise for 4x amp.
- Add sampling stage after 4x amp, to verify distortion <74dB.
- Verify specifications with dc shift.

Backup slides

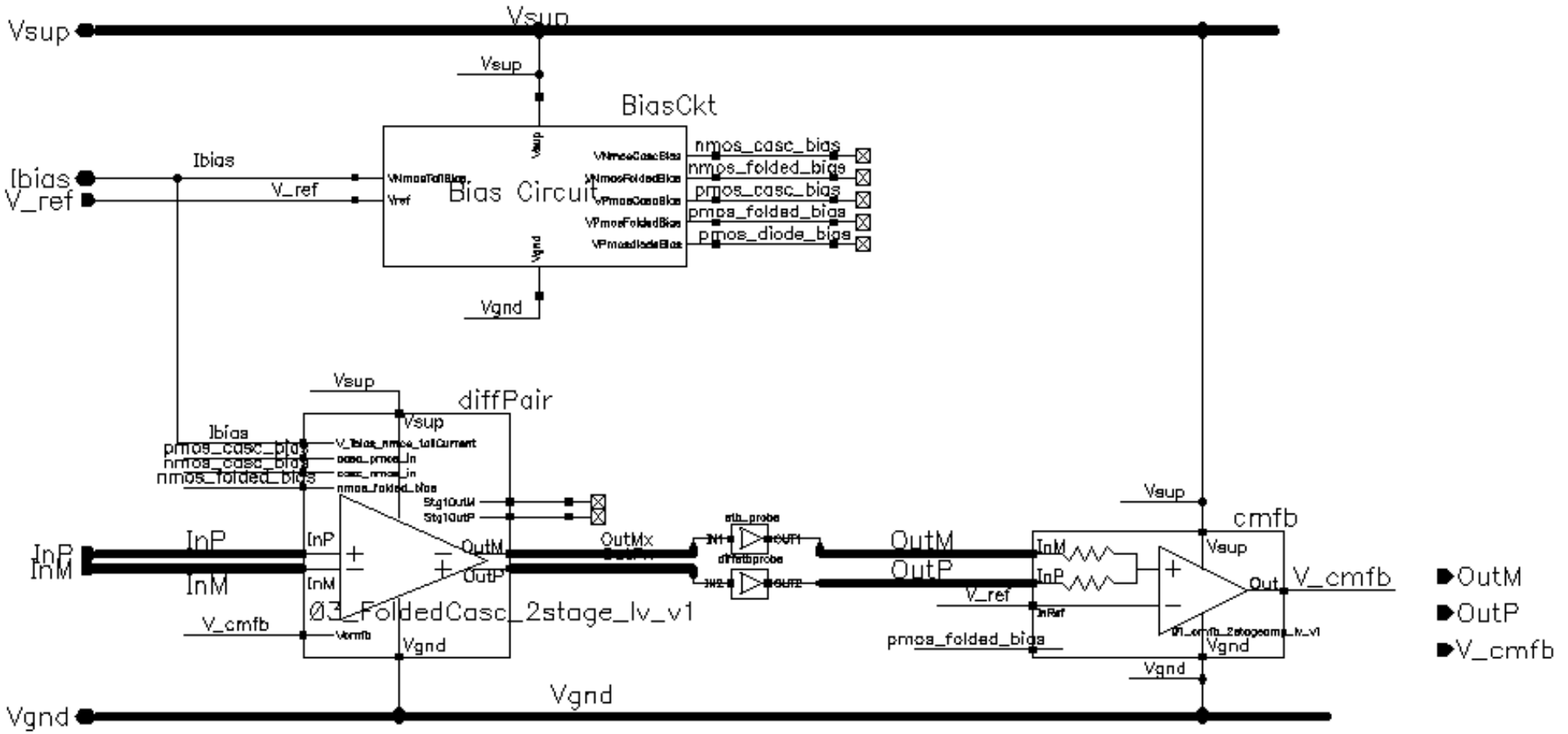
Modified multigain architecture (MMG)



CMFB schematic

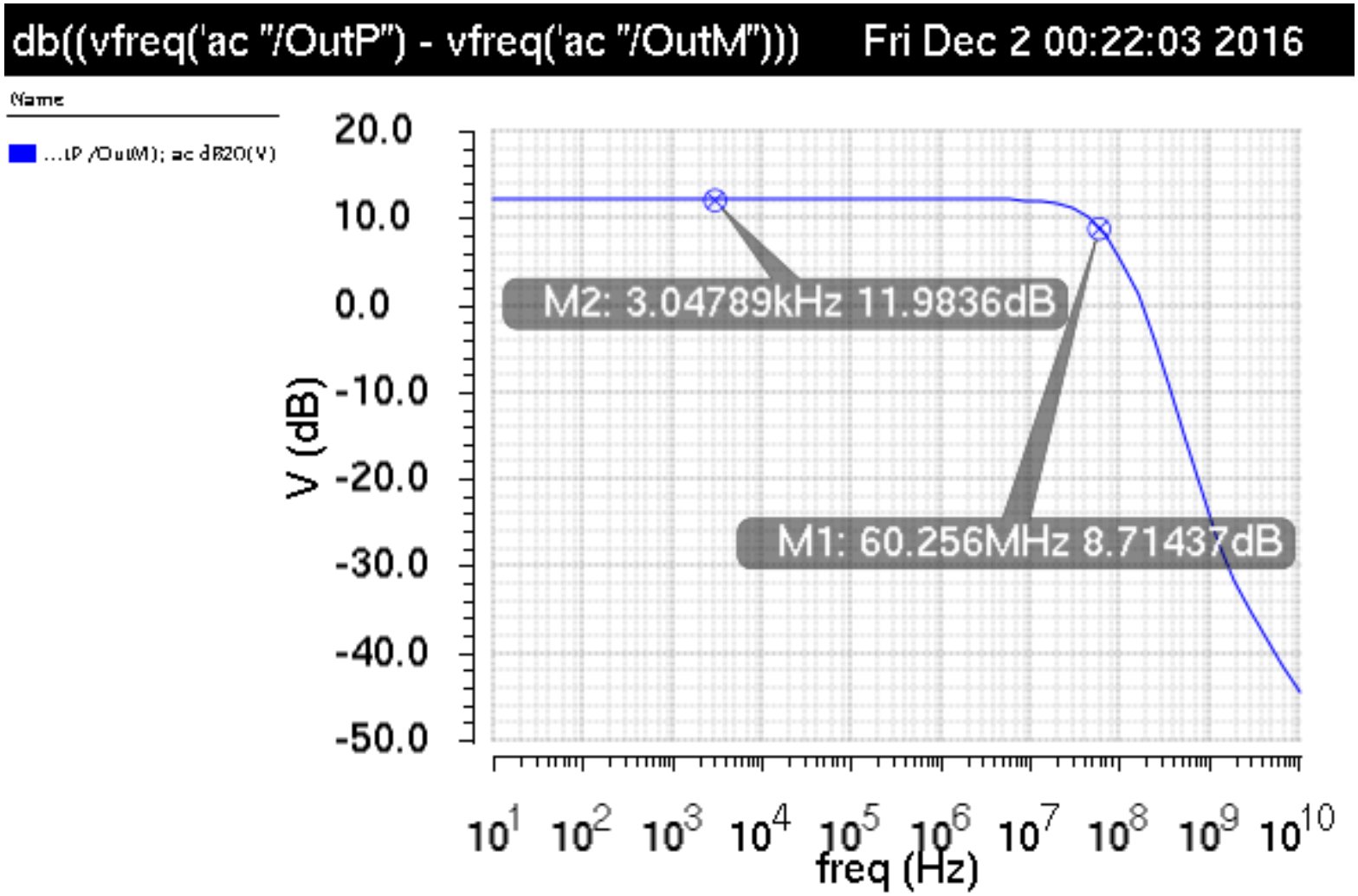


4x Amp schematic Level 1

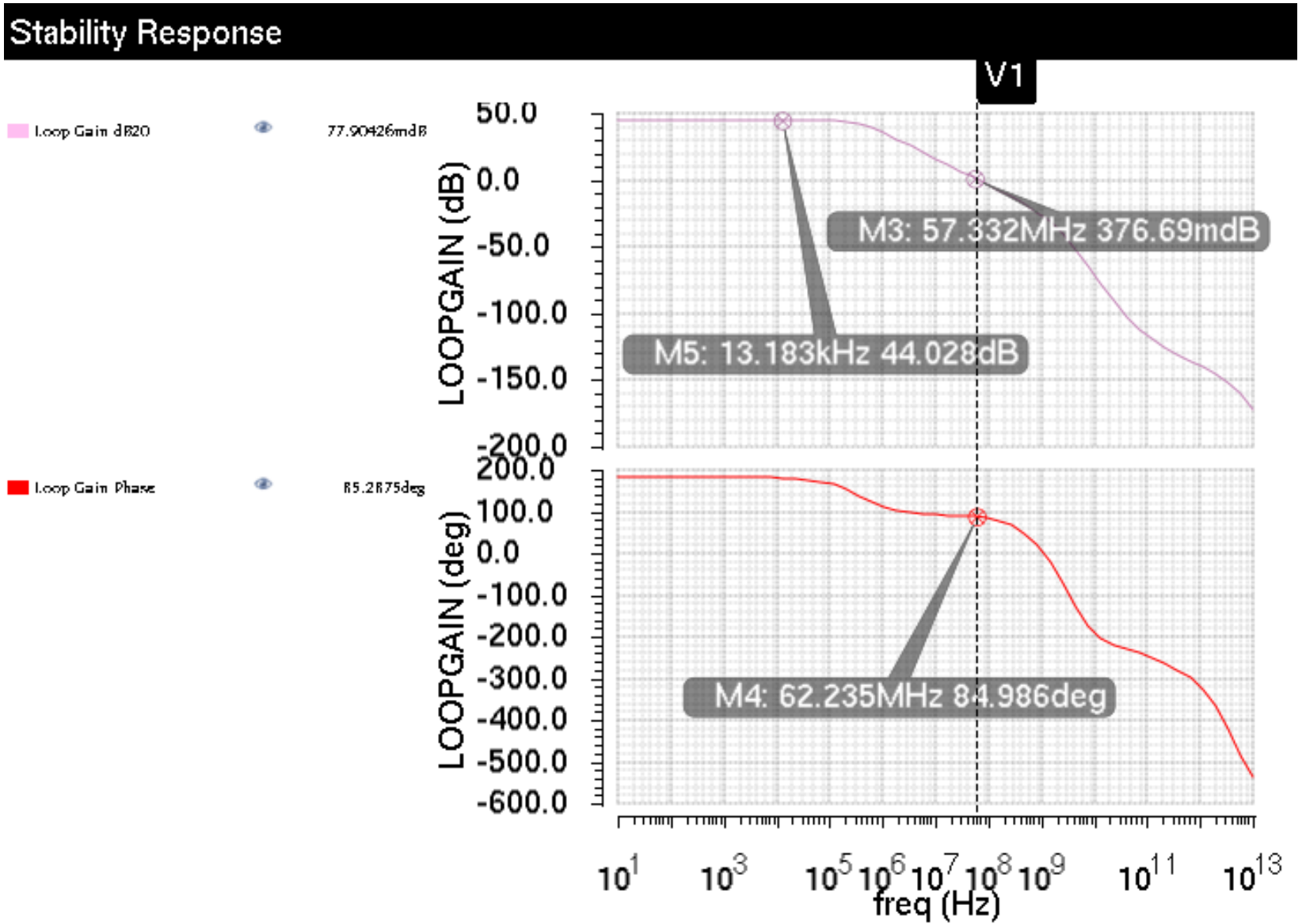


Simulation Results

AC response


db((vfreq('ac "/OutP") - vfreq('ac "/OutM")))
Fri Dec 2 00:22:03 2016
Name
...tP /OutM); ac dB20(V)
20.0
10.0
0.0
-10.0
-20.0
-30.0
-40.0
-50.0
V (dB)
M2: 3.04789kHz 11.9836dB
M1: 60.256MHz 8.71437dB
10^1 10^2 10^3 10^4 10^5 10^6 10^7 10^8 10^9 10^10
freq (Hz)

DC Loop Gain


Stability Response
V1
Loop Gain dB20
77.90426mdB
Loop Gain Phase
85.2875deg
LOOPGAIN (dB)
50.0
0.0
-50.0
-100.0
-150.0
-200.0
M3: 57.332MHz 376.69mdB
M5: 13.183kHz 44.028dB
LOOPGAIN (deg)
200.0
100.0
0.0
-100.0
-200.0
-300.0
-400.0
-500.0
-600.0
M4: 62.235MHz 84.986deg
10^1 10^3 10^5 10^6 10^7 10^8 10^9 10^11 10^13
freq (Hz)

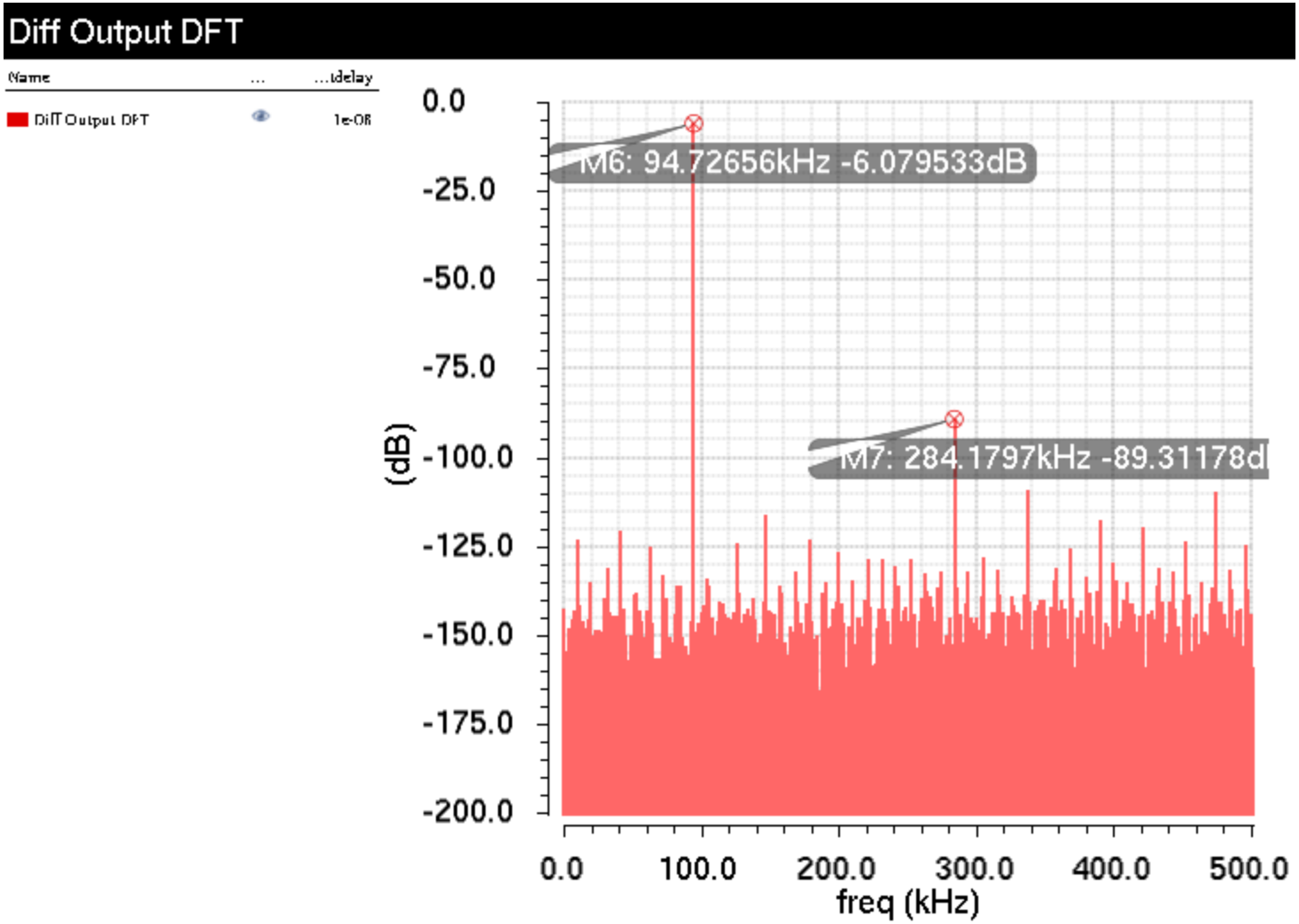
Noise Summary

Window Expressions Info Help cadence

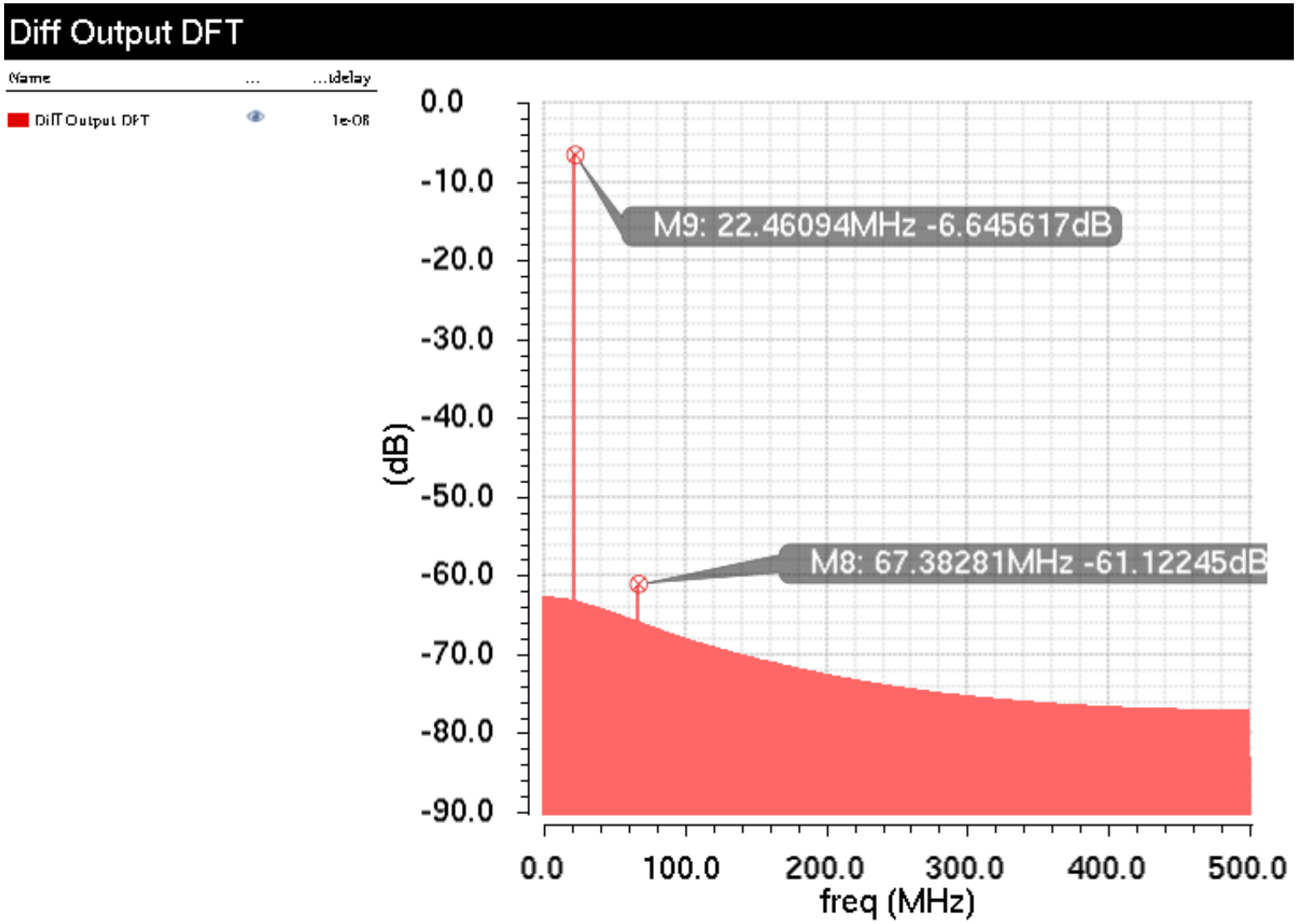
Device	Param	Noise Contribution	% Of Total
/4xAmp/diffPair/P1_bias_m	id	0.000175833	13.87
/4xAmp/diffPair/P2_bias_p	id	0.000175833	13.87
/4xAmp/diffPair/N3_folded_bias_m	id	0.000137075	8.43
/4xAmp/diffPair/N4_folded_bias_p	id	0.000137075	8.43
/4xAmp/diffPair/N1_gain_p	id	0.00011648	6.09
/4xAmp/diffPair/N2_gain_m	id	0.00011648	6.09
/R0	rn	0.000101366	4.61
/R1	rn	0.000101366	4.61
/R2	rn	0.000101366	4.61
/R3	rn	0.000101366	4.61
/4xAmp/diffPair/N2_gain_m	fn	0.000100565	4.54
/4xAmp/diffPair/N1_gain_p	fn	0.000100565	4.54
/4xAmp/diffPair/N3_folded_bias_m	fn	8.93882e-05	3.59
/4xAmp/diffPair/N4_folded_bias_p	fn	8.93882e-05	3.59
/4xAmp/diffPair/P1_bias_m	fn	5.67949e-05	1.45
/4xAmp/diffPair/P2_bias_p	fn	5.67949e-05	1.45
/R6	rn	5.00758e-05	1.13
/R5	rn	5.00758e-05	1.13
/4xAmp/diffPair/N3_stg2_OutM	id	3.18445e-05	0.46
/4xAmp/diffPair/N4_stg2_OutP	id	3.18445e-05	0.46
/4xAmp/diffPair/P3_stg2_OutM	id	3.1124e-05	0.43
/4xAmp/diffPair/P4_stg2_OutP	id	3.1124e-05	0.43
/4xAmp/diffPair/P3_folded_m	id	2.20505e-05	0.22
/4xAmp/diffPair/P4_folded_p	id	2.20505e-05	0.22
/4xAmp/diffPair/N3_folded_bias_m	rs	1.69187e-05	0.13
/4xAmp/diffPair/N4_folded_bias_p	rs	1.69187e-05	0.13
/4xAmp/diffPair/P1_bias_m	rs	1.55045e-05	0.11
/4xAmp/diffPair/P2_bias_p	rs	1.55045e-05	0.11
/4xAmp/diffPair/N1_gain_p	rs	1.49504e-05	0.10
/4xAmp/diffPair/N2_gain_m	rs	1.49504e-05	0.10

Integrated Noise Summary (in V) Sorted By Noise Contributors
Total Summarized Noise = 0.000472062
No input referred noise available
The above noise summary info is for noise data

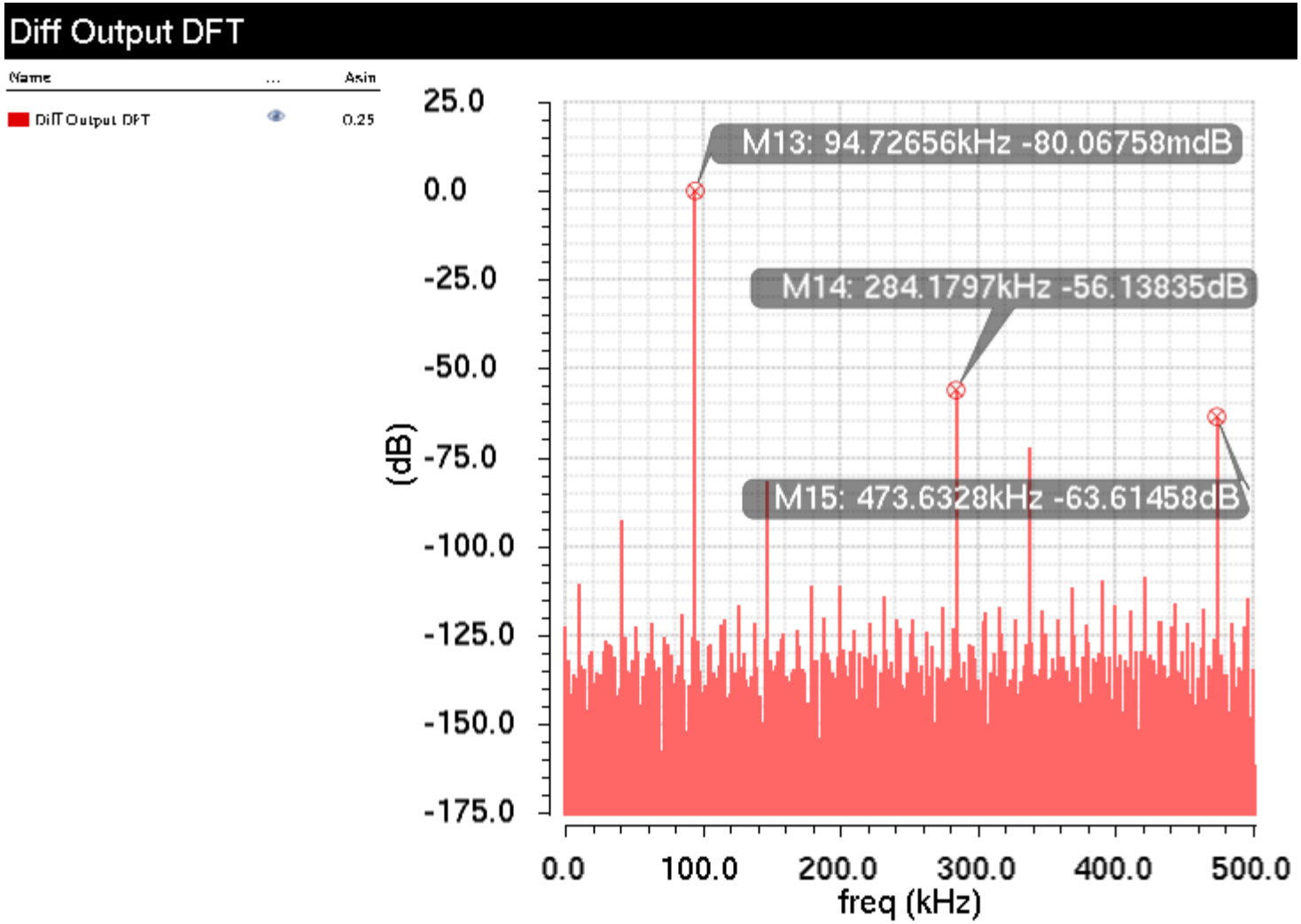
FFT $1V_{PP}$ 94.7kHz



FFT $1V_{PP}$ 22.46MHz



FFT $2V_{PP}$ 94.7kHz



FFT $2V_{PP}$ 22.46MHz